IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method of testing an integrated circuit, said method comprising:

scanning in a first plurality of bits sequentially on a pin into a first register, said first plurality of bits forming a first test code and each one of the first plurality of bits represent a corresponding ones of a first plurality of test to be performed and further indicating whether the corresponding one of the first plurality of test is to be performed ~~which indicates the specific ones of a plurality of tests to be performed; and~~

loading the first plurality of bits from said first register into a second register;

using an output of the second register, performing specific ones of the first plurality of tests indicated by each one of the first plurality of bits; and

scanning in a second plurality of bits sequentially on the pin into the first register while performing specific ones of the first plurality of tests, the second plurality of bits forming a second test code and each one of second plurality of bits represent a corresponding ones of a second plurality of test to be performed and further indicating whether the corresponding one of the second plurality of test is to be performed.

~~performing said specific ones of said plurality of tests in parallel.~~

Claims 2 – 4 (Canceled).

Claim 5 (Currently Amended): The method of claim [[4]] 1, wherein said scanning scans a plurality of control bits on said pin, said plurality of control bits representing control signals associated with said plurality of tests.

Claim 6 (Currently Amended): The method of claim 5, wherein said scanning scans some bits of said first and second test codes on a first pin and some other bits of said first and second test codes on a second pin, wherein said pin corresponds to one of said first pin and said second pin.

Claim 7 (Currently Amended): A tests enabler block reducing a number of pins required to test an integrated circuit, said tests enabler block being ~~contained~~ included in said integrated circuit, said tests enabler block comprising:

~~a first pin receiving a plurality of bits sequentially, said plurality of bits forming a test code which indicates the specific ones of a plurality of tests to be performed to test said integrated circuit.~~

a first pin for receiving a first plurality of bits sequentially the first plurality of bits forming a first test code and each one of the first plurality of bits represent a corresponding ones of a first plurality of test to be performed and further indicating whether the corresponding one of the first plurality of test is to be performed

a first register configured to serially receive the first plurality of bit from the first pin;

a second register configured to receive the first plurality of bits in parallel from the first register;

wherein the test block is further configured to use an output of the second register to perform specific ones of the first plurality of tests indicated by each one of the first plurality of bits while scanning in a second plurality of bits sequentially on the first pin into the first register the second plurality of bits forming a second test code and each one of second plurality of bits represent a corresponding ones of a second plurality of test to be performed and further indicating whether the corresponding one of the second plurality of test is to be performed.

Claims 8 – 9 (Canceled).

Claim 10 (Currently Amended): The tests enabler block of claim [[9]] **7**, ~~further comprises~~ wherein the first register is a shift register into which said plurality of bits are shifted in sequentially after being received by said first pin.

Claim 11 (Canceled).

Claim 12 (Currently Amended): The tests enabler block of claim [[11]] **10**, further comprises:

a second pin for receiving a status signal indicating whether said integrated circuit is to be operated in a test state or a functional state;

a plurality of phase pins for receiving a plurality of phase signals, wherein said plurality of phase signals operate said shift register in a shift phase in which said plurality of bits are scanned into said shift register, said plurality of phase signals operate said ~~first~~ second register in a load phase in which said plurality of bits are loaded from said shift register to said ~~first~~ second register.

Claim 13 (Canceled).

Claim 14 (Currently Amended): The tests enabler block of claim [[13]] **12**, wherein said first pin receives a plurality of control bits sequentially, said plurality of control bits representing control signals associated with said plurality of tests.

Claim 15 (Original): The tests enabler block of claim 14, wherein some bits of said test code are scanned in on a third pin and some other bits of said test code are scanned in on a fourth pin, wherein said first pin corresponds to one of said third pin and said fourth pin.